I claim:

1. A method for transforming a logical hierarchy associated with a model of an electronic design into a physical hierarchy optimized for chip-level implementation of that electronic design, the method comprising:

partitioning the model into a number of data-flow-logic partitions and control logic partitions, each partition having a boundary; and

selectively readjusting partition boundaries in response to placement based information thereby forming a physical hierarchy based on connectivity between partitions.

2. A method for partitioning an electronic design into a number of data-flow-logic partitions, the method comprising:

traversing the electronic design to group data operators inter-connected by buses into data-flow-logic partitions, wherein data operators inter-connected by an independent bus system form an independent data-flow partition; and

selectively breaking or merging each of the data-flow-logic partitions based on placement-based information.